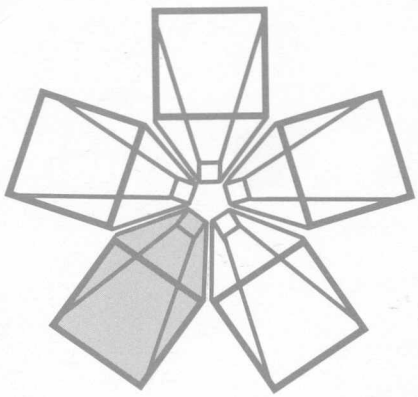
8274
MULTIPLE-PROTOCOL SERIAL CONTROLLER REFERENCE CARD



DATA COMMUNICATIONS CONTROLLERS

intel®

ORDER NO: 210514-001

8274 PROGRAMMABLE REGISTERS

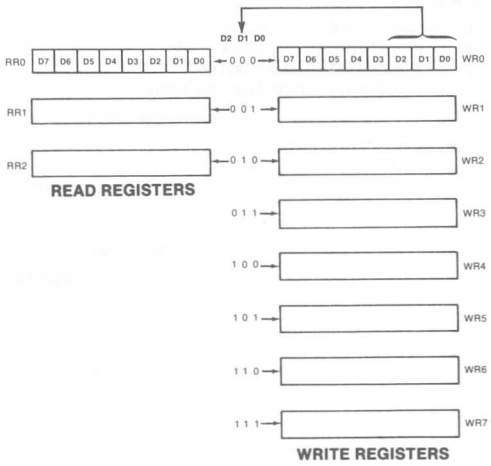
THE 8274 HAS A TOTAL OF 21 READ/WRITE REGISTERS. THE BREAKDOWN IS SHOWN IN FIGURE 1.

REGISTER TYPE	CHANNEL A	CHANNEL B
WRITE REGISTER	WR0–7	WR0–7
READ REGISTER	RR0, RR1	RR0, RR1, RR2

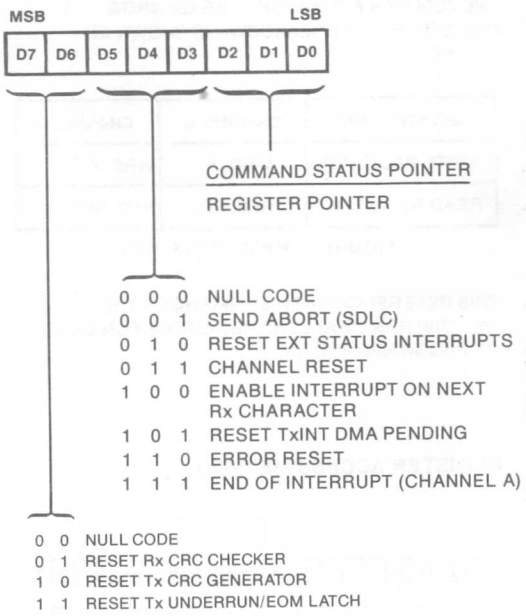
FIGURE 1. MPSC REGISTERS

THIS REFERENCE CARD SUMMARIZES THE DESCRIPTION OF ALL THE REGISTERS FOR EASE OF PROGRAMMABILITY.

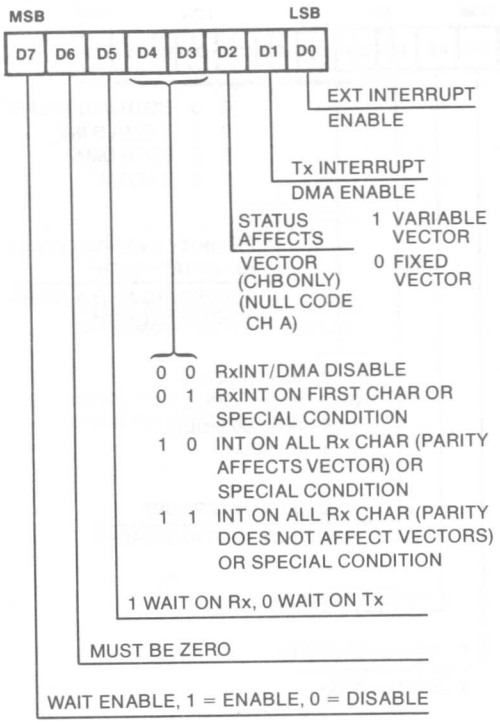
REGISTER ACCESS METHOD



WRITE REGISTER 0 (WR0):

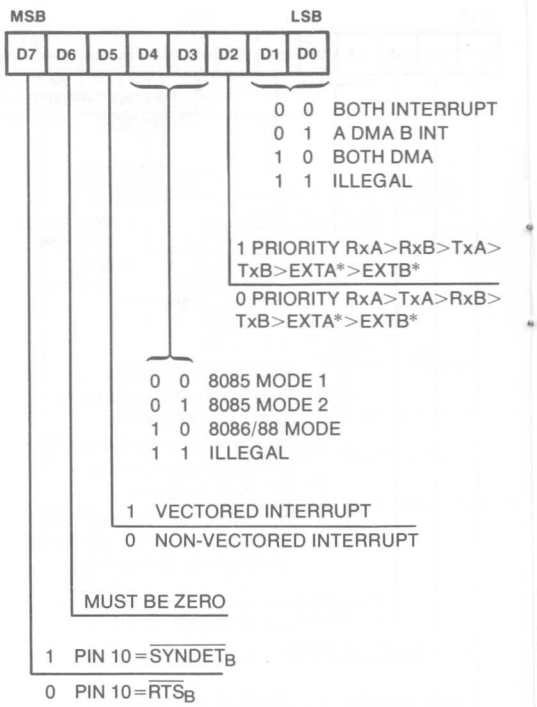


WRITE REGISTER 1 (WR1):



D2 MUST BE '0' WHEN PROGRAMMING WRI FOR CHANNEL A.

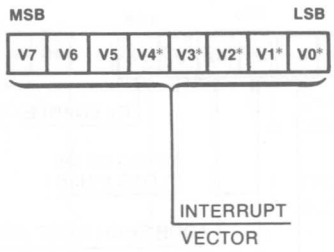
WRITE REGISTER 2(WR2): CHANNEL A



*** EXTERNAL STATUS INTERRUPT ONLY IF EXT INTERRUPT ENABLE (WR1:D0) IS SET**

NOTE: THIS REGISTER CAN BE ACCESSED THROUGH CHANNEL A ONLY.

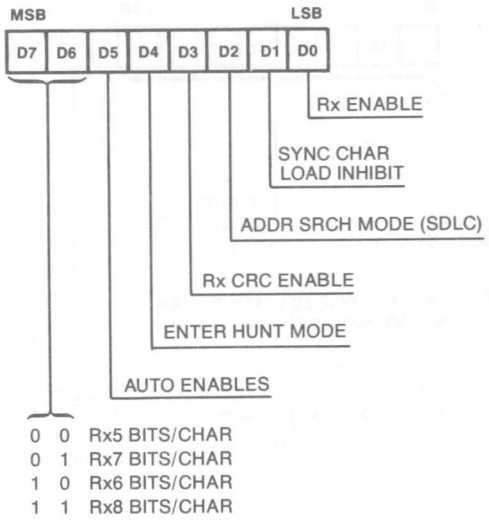
WRITE REGISTER 2 (WR2): CHANNEL B



***V4V3V2 MODIFIED IN 8085 SYSTEM**
V2V1V0 MODIFIED IN 8086 SYSTEM

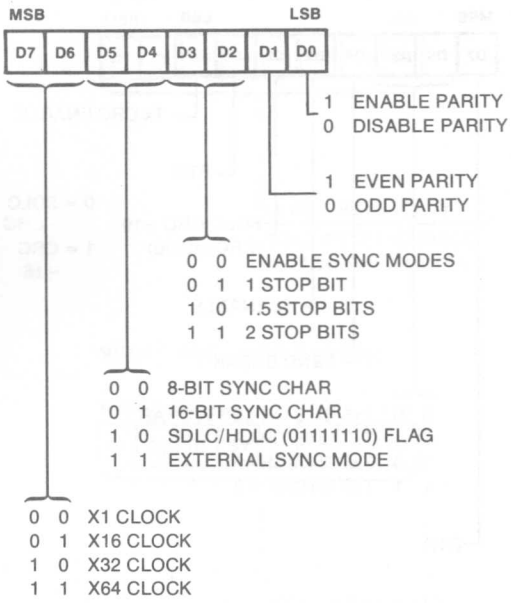
NOTE: THIS REGISTER CAN BE ACCESSED THROUGH CHANNEL B ONLY.

WRITE REGISTER 3 (WR3):

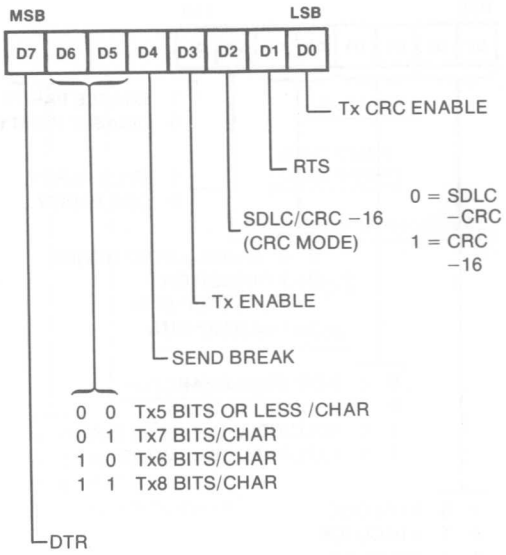


D1 MUST BE ZERO IN SDLC/HDLC MODE.

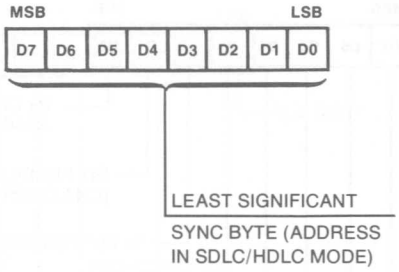
WRITE REGISTER 4 (WR4):



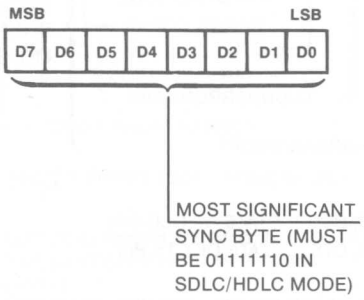
WRITE REGISTER 5 (WR5):



WRITE REGISTER 6 (WR6):



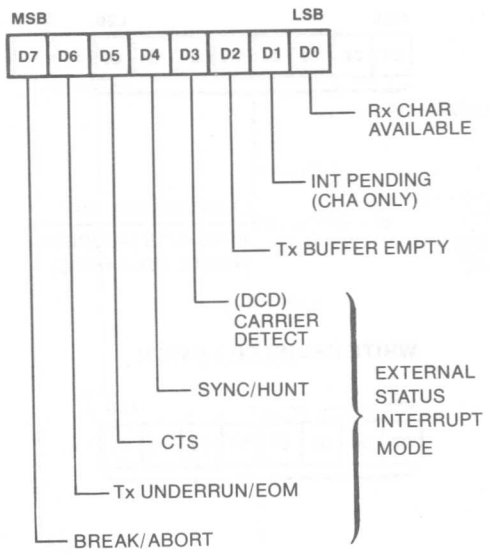
WRITE REGISTER 7 (WR7):



WR6: SHOULD CONTAIN ADDRESS BYTE IN SDLC/HDLC MODE. IN SYNC MODES, IT SHOULD CONTAIN THE LEAST SIGNIFICANT BYTE OF THE TWO SYNC BYTES.

WR7: SHOULD CONTAIN SDLC FLAG (7EH) IN SDLC/HDLC MODE. IN SYNC MODES, IT SHOULD CONTAIN THE MOST SIGNIFICANT BYTE OF THE TWO SYNC BYTES.

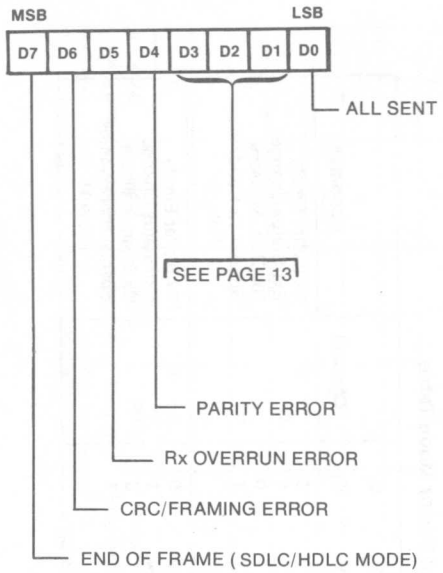
READ REGISTER 0 (RR0):



BIT D3, DCD = $\overline{\text{STATE OF DCD PIN}}$
BIT D5, CTS = $\overline{\text{STATE OF CTS PIN}}$

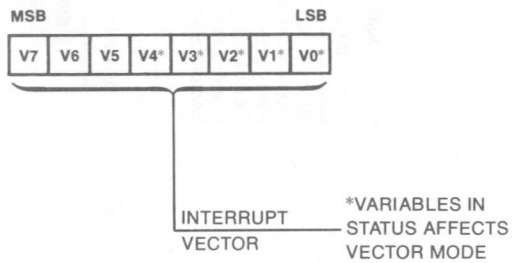
A TRANSITION ON CTS, DCD PINS GENERATES AN EXTERNAL STATUS INTERRUPT. A READ OF RR0 BEFORE ISSUING A RESET EXTERNAL STATUS COMMAND CALL INDICATE THE STATE OF DCD, CTS PINS BEFORE THE TRANSITION.
A READ OF RR0 AFTER RESET EXTERNAL STATUS COMMAND WILL INDICATE THE STATUS OF CTS/DCD PINS AFTER THE TRANSITION.

READ REGISTER 1 (RR1): (SPECIAL RECEIVE CONDITION MODE)



D0 IS VALID IN ASYNC MODE ONLY AND GETS SET AFTER THE LAST STOP BIT HAS BEEN TRANSMITTED.

READ REGISTER 2 (RR2):



Interrupt Vector Mode Table

8085 Modes 8086/88 Mode	V_4 V_2	V_3 V_1	V_2 V_0	Channel	Condition
Note 1: Special Receive Condition = Parity Error, Rx Overrun Error, Framing Error, End of Frame (SDLC)	0 0 0 0	0 0 1 1	0 1 0 1	B	Tx Buffer Empty Ext/Status Change Rx Char. Available Special Rx Condition (Note 1)
	1 1 1 1	0 0 1 1	0 1 0 1	A	Tx Buffer Empty Ext/Status Change Rx Char. Available Special Rx Condition (Note 1)

SDLC Residue Code Table (I Field Bits in 2 Previous Bytes)

RR1			8 Bits/Char		7 Bits/Char		6 Bits/Char		5 Bits/Char	
D3	D2	D1	Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte
1	0	0	0	3	0	2	0	1	0	5
0	1	0	0	4	0	3	0	2	0	1
1	1	0	0	5	0	4	0	3	0	2
0	0	1	0	6	0	5	0	4	0	3
1	0	1	0	7	0	6	0	5	—	—
0	1	1	0	8	0	—	—	—	—	—
1	1	1	1	8	—	—	—	—	—	—
0	0	0	2	8	1	7	0	6	0	4